

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Cancelled)
2. (Previously Presented) The device of claim 5, wherein said device is a memory device.
3. (Original) The device of claim 2, wherein said memory device is at least one of a static random access memory (SRAM), a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a DDR I device, a DDR II device, a Rambus DRAM (RDRAM), and a FLASH memory.
4. (Cancelled)
5. (Previously Presented) A device, comprising:
 - a delay lock loop configured to provide an output signal based upon a phase difference between a reference signal and a feedback signal, said delay lock loop comprising:
 - a coarse delay unit configured to provide a coarse delay upon at least one of said reference signal and a data output signal;
 - a fine delay unit configured to provide a fine delay upon at least one of said reference signal and said data output signal, said fine delay unit comprising:
 - a first inverter configured to invert an input signal;
 - an N-channel transistor set operatively coupled to said first inverter, said N-channel transistor set comprising a first and a second N-channel transistor, wherein a source terminal of said first N-channel transistor is coupled to a source terminal of said

second N-channel transistor and a drain terminal of said first N-channel transistor is coupled to a drain terminal of said second N-channel transistor;

a P-channel transistor set comprising a first and a second P-channel transistor, wherein a source terminal of said first P-channel transistor is coupled to a source terminal of said second P-channel transistor and a drain terminal of said first P-channel transistor is coupled to a drain terminal of said second P-channel transistor; and

a second inverter operatively coupled to said P-channel transistor, said second inverter configured to provide a complementary control signal for said P-channel transistor set;

a phase detector configured to detect said phase difference; and

a feedback delay unit operatively coupled to said coarse delay unit, said fine delay unit, and said phase detector, said feedback delay unit configured to provide a delay upon said output signal to generate said feedback signal.

6. (Previously Presented) The device of claim 5, wherein activation of at least one of said P-channel and said N-channel transistor sets provides a switching on of said capacitive delay upon said input signal to provide a delayed output signal.

7. (Previously Presented) The device of claim 5, wherein de-activation of at least one of said P-channel and said N-channel transistor sets provides a switching off of said capacitive delay upon said input signal to provide an output signal with less delay.

8. (Original) The device of claim 5, further comprising a plurality of N-channel transistor sets and P-channel transistor sets to provide additional delays upon said input signal to provide a delayed output signal.

9. (Previously Presented) The device of claim 5, wherein said output signal comprises said coarse delay and said fine delay.

10. (Previously Presented) The device of claim 5, wherein said reference signal is a clock signal.

11-25 (Cancelled)

26. (Previously Presented) The system board described in claim 29, wherein said memory location is at least one of an SRAM, a DRAM, a DDR SDRAM, a DDR I device, a DDR II device, a RDRAM, and a FLASH memory.

27. (Previously Presented) The system board of claim 29, wherein said system board is a motherboard of a computer system.

28. (Cancelled)

29. (Previously Presented) A system board, comprising:
a first device comprising a memory location for storing data and a delay lock loop configured to provide an output signal based upon a phase difference between a reference signal and a feedback signal, the delay lock loop comprising:

a coarse delay unit configured to provide a coarse delay upon at least one of said reference signal and a data output signal;

a fine delay unit configured to provide a fine tuned delay upon at least one of said reference signal and said data output signal, said fine delay unit comprising:

a first inverter to invert an input signal;

an N-channel transistor set operatively coupled to said first inverter, said N-channel transistor set comprising a first and a second N-channel transistor, wherein a source terminal of said first N-channel transistor is coupled to a source terminal of said second N-channel

transistor and a drain terminal of said first N-channel transistor is coupled to a drain terminal of said second N-channel transistor;

a P-channel transistor set comprising a first and a second P-channel transistor, wherein a source terminal of said first P-channel transistor is coupled to a source terminal of said second P-channel transistor and a drain terminal of said first P-channel transistor is coupled to a drain terminal of said second P-channel transistor; and

a second inverter operatively coupled to said P-channel transistor, said second inverter configured to provide a complementary control signal for said P-channel transistor set;

a phase detector configured to detect said phase difference; and

a feedback delay unit operatively coupled to said coarse delay unit, said fine delay unit, and said phase detector, said feedback delay unit configured to provide a delay upon said output signal to generate said feedback signal; and

a second device operatively coupled to said first device, said second device configured to access said data from said first device based upon an operation performed by said delay lock loop.

30. (Previously Presented) The system board of claim 29, wherein activation of at least one of said P-channel and said N-channel transistor sets provides switches on a capacitive delay upon said input signal to provide a delayed output signal.

31. (Previously Presented) The system board of claim 29, wherein de-activation of at least one of said P-channel and said N-channel transistor sets switches off a capacitive delay upon said input signal to provide an output signal with less delay.

32. (Original) The system board of claim 29, further comprising a plurality of N-channel transistor sets and P-channel transistor sets to provide additional delays upon said input signal to provide a delayed output signal.

33. (Previously Presented) The system board of claim 29, wherein said output signal comprises said coarse delay and said fine delay.

34. (Previously Presented) The system board of claim 29, wherein said reference signal is a clock signal.

35. (Cancelled)

36. (Previously Presented) The memory device of claim 39, wherein said memory device is at least one of a static random access memory (SRAM), a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a DDR I device, a DDR II device, a Rambus DRAM (RDRAM), and a FLASH memory.

37. (Cancelled)

38. (Cancelled)

39. (Previously Presented) A memory device, comprising:
a delay lock loop configured to provide an output signal based upon a phase difference between a reference signal and a feedback signal, said delay lock loop comprising:

a coarse delay unit configured to provide a coarse delay upon at least one of said reference signal and a data output signal;

a fine delay unit configured to provide a fine tuned delay upon at least one of said reference signal and said data output signal, said fine delay unit comprising:

a first inverter configured to invert an input signal;

an N-channel transistor set comprising a first and a second N-channel transistor, wherein a source terminal of said first N-channel transistor is coupled to a source terminal of said second N-channel transistor and a drain terminal of said first N-channel transistor is coupled to a drain terminal of said second N-channel transistor;

a P-channel transistor set comprising a first and a second P-channel transistor, wherein a source terminal of said first P-channel transistor is coupled to a source terminal of said second P-channel transistor and a drain terminal of said first P-channel transistor is coupled to a drain terminal of said second P-channel transistor; and

a second inverter configured to provide a complementary control signal for said P-channel transistor set;

a phase detector configured to detect said phase difference; and

a feedback delay unit operatively coupled to said coarse delay unit, said fine delay unit, and said phase detector, said feedback delay unit configured to provide a delay upon said output signal to generate said feedback signal.

40. (Previously Presented) The memory device of claim 39, wherein activation of at least one of said P-channel and said N-channel transistor sets provides a switching on of a capacitive delay upon said input signal to provide a delayed output signal.

41. (Previously Presented) The memory device of claim 39, wherein de-activation of at least one of said P-channel and said N-channel transistor sets provides a switching off of a capacitive delay upon said input signal to provide an output signal with less delay.

42. (Previously Presented) The memory device of claim 39, further comprising a plurality of N-channel transistor sets and P-channel transistor sets configured to provide additional delays upon said input signal to provide a delayed output signal.

43. (Previously Presented) The memory device of claim 39, wherein said output signal comprises said coarse delay and said fine delay.

44. (Original) The device of claim 43, wherein said reference signal is a clock signal.

45- 49. (Cancelled)